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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/087,915	03/05/2002	Yoshiyuki Tonami	36856.636	6607

7590 12/04/2002

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EXAMINER	
NADAV, ORI	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/087,915	TONAMI ET AL.	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *9,11 and 13-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of Group II, claims 1-8, 10 and 12 in Paper No. 6 is acknowledged.

Oath/Declaration

2. The oath/declaration filed on 03/05/2002 is acceptable.

Drawings

3. The formal drawings filed on 03/05/2002 are acceptable.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

5. If applicant is aware of any relevant prior art, he/she requested to cite it on form PTO-1449 in accordance with the guidelines set forth in M.P.E.P. 609.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-8, 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over in view of Kitamura et al. (5,480,048) in view of Applicant Admitted Prior Art (AAPA).

Regarding claims 1, 2 and 10, Kitamura et al. teach in figures 9a-9g and related text (column 11, line 51 to column 12, line 19) a method of producing a high frequency circuit chip having a substrate made of a ceramic (column 5, lines 18-19) with a high dielectric constant, a wiring pattern 901 provided on one main surface of the substrate and the wiring pattern disposed on each of front and back main surfaces of the substrate 207 (see figure 2i), and a through-hole 902 Including a connecting electrode for connecting the wiring pattern and the conductor layer to each other, the method comprising the steps of: Filling electrically conductive material into a perforation in the substrate, and firing the conductor to form the connecting electrode of the through-hole; forming a resist pattern 903 with an opening having a desired shape and size on the substrate; forming a thin film 904 with a wiring material on the substrate through the opening over the resist pattern after forming the resist pattern; and removing the

unnecessary wiring material thin film deposited on the resist pattern together with the resist pattern (figure 9d) to form the wiring pattern on the substrate by a lift-off method. Although figures 9a-9g do not depict a wiring material over the resist pattern, it is well known in the art that a wiring material is deposited on the entire surface of the substrate, including the resist pattern. Therefore, Kitamura et al. teach a wiring material being deposited on the entire surface of the substrate, including the resist pattern, as claimed. In the alternative, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to deposit the wiring material on the entire surface of the substrate, including the resist pattern in Kitamura et al.'s device in order to simplify the processing steps of making the device.
Kitamura et al. do not teach using a conductive paste. AAPA teaches in figure 8 and related text a conductive paste 60. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use conductive paste in Kitamura et al.'s device in order to pattern and manipulate the conductive material with more ease.

Regarding claims 1 and 7, Kitamura et al. teach in figure 17 an electric conductor layer 1705 provided on substantially all of another main surface of the substrate. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an electric conductor layer on substantially all of another main surface of

the substrate in Kitamura et al.'s device, in order to use the device in an application which requires a contact electrode on the bottom of the substrate.

Regarding claim 3, Kitamura et al. teach in figure 9e forming a protection film 905 so as to cover the wiring pattern on the substrate. Kitamura et al. do not disclose cutting the substrate along desired dicing lines to obtain the high frequency circuit. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to cut the substrate along desired dicing lines to obtain the high frequency circuit in order to obtain an operative device.

Regarding claim 4, AAPA teaches in figure 8 forming a thin-film resistor pattern 55 which is connected to the wiring pattern.

Regarding claim 5, Kitamura et al. teach a mirror-polishing at least the surface of the fired substrate on which the wiring pattern is formed, and the fired substrate in which the through-hole having the connecting electrode is formed, and thereafter forming the wiring pattern on the mirror-polished surface by the lift-off method.

Regarding claim 6, Kitamura et al. teach a ceramic substrate having a relative dielectric constant of at least about 10.

Regarding claims 7, 8 and 12, Kitamura et al. and AAPA teach the wiring pattern formed on at least one main surface of the substrate and the electric conductor layer formed on substantially all of the other main surface by a conductor pattern containing at least one metal selected from the group consisting of AG, Cu, and Al as a major component and having a thickness of at least about 2 microns (Kitamura et al., column 12, line 44), wherein a connecting electrode of the through-hole is formed by including at least one metal selected from the group consisting of AG, Cu, and Al as a major component.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached at **(703) 308-2772.**

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

Ori Nadav

December 2, 2002